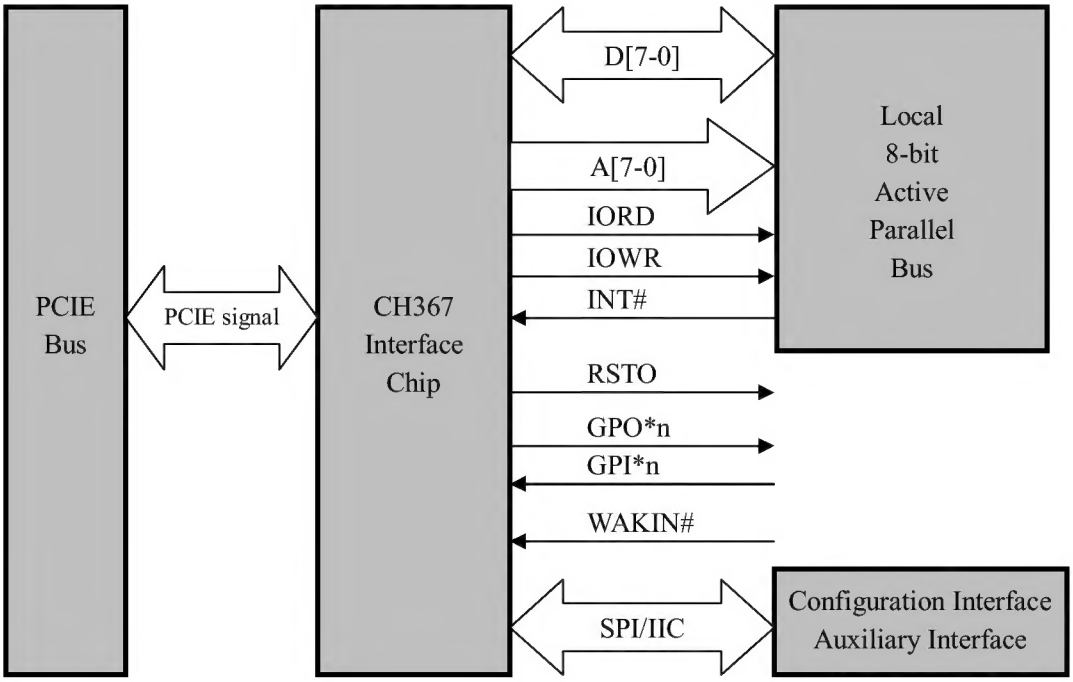
PCIE Bus Interface Chip CH367

Datasheet
Version: 1B
http://wch.cn

1. Introduction

CH367 is a general interface chip based on PCI-Express bus, supports I/O port mapping, expansion ROM and interrupt. CH367 converts high-speed PCIE bus into an easy-to-use 8-bit active parallel interface which is similar to ISA bus, for making low-cost computer board card based on PCIE bus and upgrading the original board card based on ISA bus or PCI bus onto PCIE bus. Compared with other mainstream buses, PCIE bus has higher speed, better real-time and controllability, so CH367 is suitable for high-speed real-time I/O control card, communication interface card, data acquisition card, etc.

The figure below shows its general application block diagram.

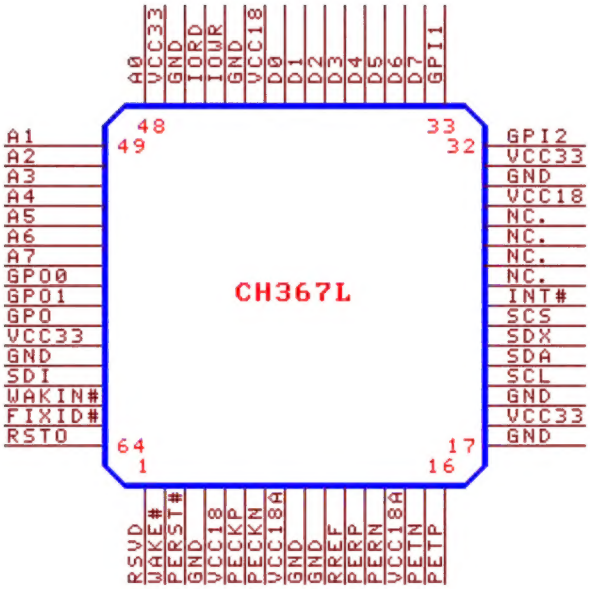


2. Features

- Provides 8-bit active parallel bus based on PCIE bus.
- Supports I/O read and write, automatic allocation of I/O base address, and supports I/O port up to 232bytes.
- Read and write pulse width is selectable from 30nS to 450nS, and the access speed can reach 1MB/s.
- Supports request input of level interrupt or edge interrupt, interrupt sharing.
- Supports flash memory expands ROM without hard disk boot, and provides the sub-program library BRM of expanding ROM application.
- Provides high-speed 3-wire or 4-wire SPI serial host interface.
- Provides two-wire serial host interface, which can connects serial-port EEPROM device 24C0X to store non-volatile data.
- The device identification (Vendor ID, Device ID, Class Code, etc.) of the PCIE board can be set in the EEPROM device.
- Built-in 2uS to 8mS hardware timing unit, used as a delay reference during software running.

- Drive supports Windows 98/ME/NT4.0/2000/XP/Vista/7+ and Linux, and provides application layer API through DLL.
- 3.3V supply voltage, I/O pins supports 5V withstand voltage, and low-power sleep mode.
- Supports PCMCIA of ExpressCard notebook card.
- RoHS compliant and LQFP-64 lead-free package.

3. Package



Package	Width Of Plastic	Pitch Of Pin		Instruction Of Package	Ordering Information
LQFP-64	7mm x 7mm	0.4mm	15.7mil	Small outline LQFP64 pin patch	CH367L

4. Pin Out

4.1. Power Line

Pin No.	Pin Name	Type	Pin Description
18,31,47,59	VCC33	Power	3.3V I/O power
5,29,42	VCC18	Power	1.8V core power
8,14	VCC18A	Power	1.8V transmission power
4,9,10,17,19,30,43,46,60	GND	Power	Ground
25,26,27,28	NC.	None	No connection

4.2. PCIE Bus Signal Line

Pin No.	Pin Name	Type	Pin Description
3	PERST#	Input	System reset signal lines, active low
6,7	PECKP/PECKN	Input	System reference clock differential input
12,13	PERP/PERN	PCIE input	Differential signal input of PCIE receiver
16,15	PETP/PETN	PCIE output	Differential signal output of PCIE transmitter
2	WAKE#	Open-drain output	Bus wake-up output, active low, not connected if not used

4.3. Local Terminal Signal Line

Pin No.	Pin Name	Type	Pin Description
34-41	D7~D0	Tri-status output and input	8-bit bi-directional data signal line, built-in pull-up resistor
55-48	A7~A0	Output	8-bit address signal line
45	IORD	Output	Read strobe of I/O port, active low-level pulse
44	IOWR	Output	Write strobe of I/O port, active low-level pulse
24	INT#	Input	Interrupt request input, active level or edge, built-in pull-up resistor

4.4. Auxiliary Signal Line

Pin No.	Pin Name	Type	Pin Description
11	RREF	Input	System reference current input; connected a external 12KΩ resistor to GND
20	SCL	Output	General output, SPI clock output, clock output of external configuration chip, connected SCL pin of the serial EEPROM configuration chip 24CXX externally
21	SDA	Open-drain output and input	General output and input, built-in pull-up resistor, connected SDA pin of the serial EEPROM configuration chip 24CXX externally
22	SDX	Tri-status and bi-direction	General output and input, SPI data output and input, built-in pull-up resistor
23	SCS	Output	General output, SPI chip selection output
61	SDI	Input	General input, SPI data input, built-in pull-up resistor
33	GPI1	Input	General input, built-in pull-up resistor
32	GPI2	Input	General input, built-in pull-up resistor
56	GPO0	Output	General output, low level by default
57	GPO1	Output	General output, low level by default
58	GPO	Output	General output, high level by default
64	RSTO	Output	Reset output at active low, general output
62	WAKIN#	Input	Wake-up request input, active low, connected to high level if not used
63	FIXID#	Input	Disable automatic loading of identification information input, active low, built-in pull-up
1	RSVD	Reserved	Reserved, no connection

5. Registers

5.1. Basic Specification

5.1.1. Abbreviation of Attribute: R=read-only, W=read and write, S=read-only but can be set in advance,….=ellipsis.

5.1.2. Numerical system of data: If it ends with H which is a hexadecimal number. Otherwise, it is a binary number.

5.1.3. Wildcard character and attribute of numeric value: r=reserved (disabled), x=any value, ...=ellipsis.

5.2. PCIE Configuration Space

Address	Register Name	Register Attribute	Default Value After System Reset
01H-00H	Vendor ID	SSSS	1C00H
03H-02H	Device ID	SSSS	SDI is high when reset: 5831H SDI is low when reset: 5830H
05H-04H	Command	RRRRRWRWRWRRRWWW	0000000000000000
07H-06H	Status	RRRRRRRRRRRRRRRR	000000000001x000
08H	Revision ID	SS	10H
0BH-09H	Class Code	SSSSSS	100000H
0FH-0CH		RRRRRRWW	00000000H
13H-10H	I/O Base Address	WWWWWWRR	00000001H
2BH-14H		RRRR….RRRR	0000….0000H
2DH-2CH	Sub-system Vendor ID Subsystem Vendor ID	SSSS	Same as VID
2FH-2EH	Subsystem ID	SSSS	Same as DID
33H-30H	ROM Base Address	WWWWWWWWWWWWWWWW WRRRRRRRRRRRRRRW	0000000000000000 0000000000000000
3BH-34H		RRRR….RRRR	0000….0060H
3FH-3CH	Interrupt Line & Pin	RRRRRRRRRRRRRRRR RRRRRRRRWWWWWWWW	0000000000000000 0000000100000000
FFFH-40H	Reserved	(Disabled)	(Disabled)

5.3. I/O Base Address Register

The actual address of the register is the I/O base address plus the offset address in the table.

Offset Address	Register Name	Abbreviation	Register Attribute	Default Value After System Reset
E7H-00H	Standard local I/O port	IOXR	WW	Connect to I/O device
E8H	General output register	GPOR	WWWRRWWW	000rr111
E9H	General variable register	GPVR	WWWWWWWW	00001010
EAH	General input register	GPIR	RRRRRRRR	11r11111
EBH	Interrupt control register	INTCR	RRRWWWWR	rrr0000r
F0H-ECH	Reserved		(Disabled)	xxH
F1H	General output register 2	GPOR2	WRRRRRWW	1rrrrr00
F7H-F2H	Reserved		(Disabled)	xxH
F8H	Miscellaneous control and status registers	MICSR	WRRRRWRW	1rrr10r1
F9H	Reserved		(Disabled)	xxH
FAH	Read and write speed control register	SPDCR	RRWWWWWW	rr000111
FBH	Reserved		(Disabled)	xxH
FCH	Hardware cycle count register	CNTR	RR	xxH
FDH	SPI control register	SPICR	WWWRRRRR	0000xxxx
FEH	SPI data register	SPIDR	WW	xxH
FFH	Reserved		(Disabled)	xxH

5.4. Register Bit

Register Name	Address	Attribute	Instruction For Use Of Bit (Default Value)	Value=0	Value=1
General output register GPOR (I/O base address + 0E8H address)	Bit 0	W	Set output value of SDA pin(1)	Low	High
	Bit 1	W	Set output value of SCL pin(1)	Low	High
	Bit 2	W	Set output value of SCS pin(1)	Low	High
	Bit 5	W	Enable support is compulsorily awaked(0)	Not support	Support
	Bit 6	W	Set data direction of SDX pin(0)	Input	Output
	Bit 7	W	Set output value of SDX pin(0)	Low	High
General input register GPIR (I/O base address + 0EAH address)	Bit 0	R	Input status of SDA pin(1)	Low	High
	Bit 1	R	Input status of GPI1 pin(1)	Low	High
	Bit 2	R	Input status of GPI2 pin (1)	Low	High
	Bit 3	R	Input status of INT# pin(1)	Low	High
	Bit 4	R	Input status of WAKIN# pin(1)	Low	High
	Bit 6	R	Input status of SDI pin(1)	Low	High
	Bit 7	R	Input status of SDX pin(1)	Low	High
Interrupt control register INTCR (I/O base address + 0EBH address)	Bit 1	W	Global interrupt enabling(0)	Disable interrupt	Enable interrupt
	Bit 2	W	Polarity of INT# pin interrupt input(0)	Low Rising edge	High Falling edge
	Bit 3	W	Type of INT# pin interrupt input	level	Edge
	Bit 4	W	Interrupt request retry enabling (0)	Disable retry	Enable retry
General output register 2 GPOR2 (I/O base address + 0F1H address)	Bit 0	W	Set output value of GPO0 pin(0)	Low	High
	Bit 1	W	Set output value of GPO1 pin(0)	Low	High
	Bit 7	W	Set output value of GPO2 pin(1)	Low	High
Miscellaneous control and status registers MICSR (I/O base address + 0F8H address)	Bit 0	W	Set output value of GPO3 pin(1)	Low	High
	Bit 2	W	Interrupt active status(0)	No interrupt	interrupt
	Bit 3	R	Input status of INT# pin(1)	Low	High
	Bit 7	W	Set output value of RSTO pin(1)	Low	High
Read and write speed control register SPDCR (I/O base address + 0FAH address)	Bit 0 Bit 1 Bit 2 Bit 3	WWWW	Total width of reading and writing signals including building time and keeping time (0111), the step distance is 30nS, and 0000~1111 correspond to 60nS~510nS, the total width minus the building time of bit 4 and minus the keeping time of bit 5 to get the net width of the reading and writing pulse. The minimum value is 0nS, and the maximum value is 480nS		
	Bit 4	W	Building time of data and address output(0)	15nS	45nS
	Bit 5	W	Keeping time of data and address output (0)	15nS	45nS

SPI control register SPICR (I/O base address + 0FDH address)	Bit 0 ~ bit 3	RRRR	High-order 4 bits of hardware cycle count(XXXX), totally 12 bits plus the hardware cycle count register CNTR		
	Bit 4	R	Transmitting status of SPI(0)	Idle	Transmitting
	Bit 5	W	Select the SPI serial clock frequency (0)	31.3MHz	15.6MHz
	Bit 6	W	Select the SPI data input pin (0)	SDX	SDI
	Bit 7	W	Start new transmission (0) after enabling to read SPIDR	Idle after reading	Start after reading

6. Function Descriptions

6.1. External Configuration Chip

CH367 will check the data in external 24CXX configuration chip after each power-on or PCIE bus reset. If the configuration chip is connected and the data is valid, it will be automatically loaded into CH367 to replace the default PCIE identification information.

FIXID# pin is used to set whether to check the external configuration chip. For the low level, the external configuration chip will not be checked, thereby disabling automatic loading of identification information.

24CXX is a non-volatile serial EEPROM memory which is 4-pin or 8-pin package. Except for providing configuration information to CH367, it also can self-save some other parameters for application. CH367 supports the following types of 24CXX chips: 24C01 (A), 24C02, 24C04, 24C08, 24C16, etc.

The following table shows the 24CXX data definition.

Byte Address	Abbreviation	Description Of Data Application	Default Value
00H	SIG	The valid flag of the external configuration chip, must be 78H	78H
01H	CFG	Configuration parameter	00H
03H-02H	RSVD	(Reserved unit)	0000H
05H-04H	VID	Vendor ID	Customized
07H-06H	DID	Device ID	Customized
08H	RID	Revision ID	Customized
0BH-09H	CLS	Class Code	100000H
0DH-0CH	SVID	Subsystem Vendor ID	Customized
0FH-0EH	SID	Subsystem ID	Customized
1FH-10H	RSVD	(Reserved unit)	00H or FFH
Other address	APP	User or application customs unit	

6.2. Space Mapping

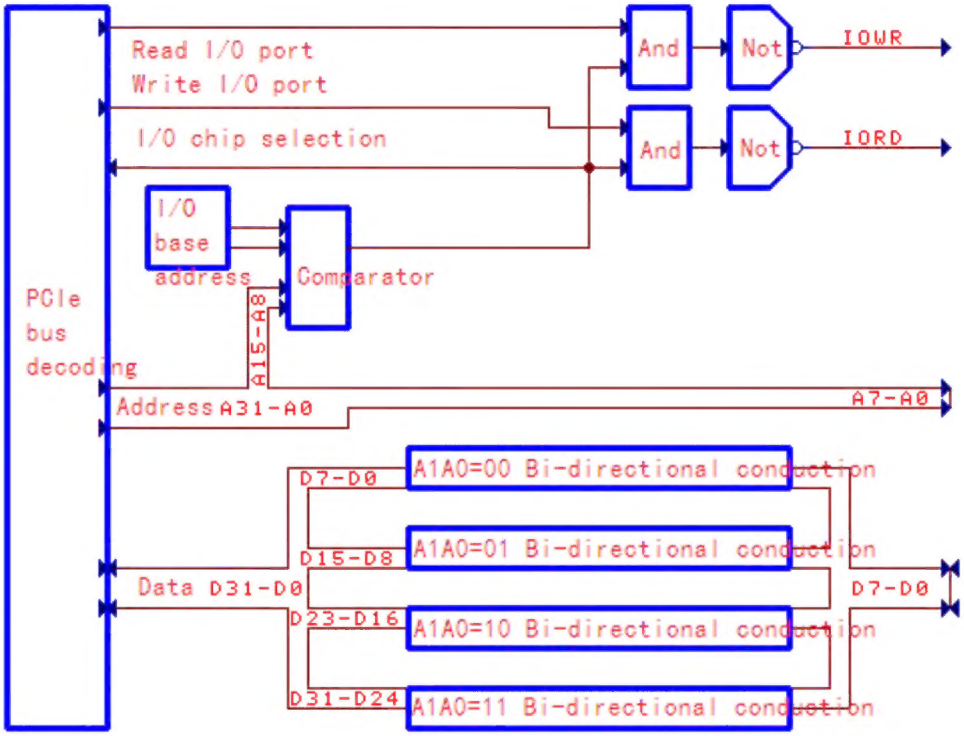
There are three types of spaces in PC: memory space, I/O space, and configuration space. The memory space, mainly including memory, video memory, expansion ROM and device buffer, etc., which is generally used to store large amounts of data and exchange data blocks. I/O space, mainly including the control register and status register of the device, which is generally used to control and query the working status of the device and exchange a small amount of data. The configuration space is mainly used to provide basic information of the device to the system, and to accept the system's control and query for the device's global status.

To avoid address conflicts, PCIE bus requires that the occupied address of each device can be relocated. Relocation is realized by the base address register of the configuration space of the device. Normally, the base address register of each device is always assigned to a different base address by BIOS or OS, so that each device is separately mapped to a different address range. When needed, the application can also modify

the base address by itself.

I/O space of CH367 occupies 256 bytes. Except for the self-use register of CH367, it also can provide 232 bytes for external device. The offset address is 00H~E7H, the actual address is I/O base address plus offset address.

6.3. Internal Structure And Signal Line



The figure above is the main structure of CH367. After CH367 decodes various signals of PCIE bus, it generates internal data buses D31~D0, internal address buses A31~A0, read I/O port signal and write I/O port signal, etc. The transmission direction of each signal has been marked in the figure.

The signal on the right side of the structure diagram refers to the external pin provided by CH367 to the local terminal. The address lines A7 ~ A0 are used to provide offset addresses relative to the base address, and the data buses D7 ~ D0 are used to input data during a reading operation, and are used to output data during a writing operation. IORD is used to provide the I/O read strobe pulse signal, IOWR is used to provide the I/O write strobe pulse signal, and the read and write strobe pulse signals of the above pins are all active at low level. The address line, data bus and the read and write strobe signal line provided by CH367 are similar to the signal line of ISA bus, so it is very suitable for upgrading ISA board onto PCIE bus. The figure indicates that the read and write strobe signals provided by CH367 have been controlled by chip selection inside the chip, and the read and write strobe signals outputted by CH367 are only valid within its base address mapping range, so the chip selection decoding is not required for the external device.

During the I/O reading and writing operations, A7~A0 of CH367 output the offset address of I/O port. The effective offset address range provided to the external device is 00H~E7H, and the external device can further decode A7~A0 to generate a secondary chip selection signal.

6.4. Data Width

CH367 supports PC program to read and write I/O port in single byte as unit. The internal register of CH367 (located at I/O base address + 0E8H and above addresses) always supports the access of PC program in unit

of single byte, double byte (character) and four bytes (double characters).

When performing double-byte access, the initial address must be arbitrary character boundary address (a multiple of 2) in the base address range; when performing four-byte access, the initial address must be arbitrary double-character boundary address in the base address range (a multiple of 4).

6.5. Hardware Interrupt

CH367 supports level or edge interrupt request input, which is selected by bit 3 of the interrupt control register INTCR, and its polarity is selected by bit 2. There are four types: active at low level, active at high level, active at rising edge and active at falling edge.

In the edge interrupt mode, after the INT# pin detects a valid edge input, the interrupt active status bit of CH367 (bit 2 of the miscellaneous control and status register MICSR) is automatically set to 1 to remember the edge and apply for interrupt to PCIE bus at the same time. After entering the interrupt service, the software must clear the interrupt activation status bit in time to cancel (end) the interrupt request.

In the level interrupt mode, after the INT# pin detects a valid level input, CH367 will directly apply for interrupt to PCIE bus. After the input level is invalid, CH367 will cancel (end) the interrupt request to PCIE bus. If it is cancelled soon after CH367 applies for interrupt to PCIE bus, the interrupt request may be ignored by the PC.

If the PC program sets the interrupt activation status bit of CH367 to 1 in the software mode, it can also enable that CH367 enters the interrupt active status, then applying for interrupt to PCIE bus. Such software interrupt has exactly the same characteristics as the hardware interrupt caused by the external input of the INT# pin, and can be used to test the interrupt function of CH367.

The standard interrupt process is as follows:

① The external circuit outputs a valid interrupt request signal to INT# pin.
② CH367 applies for interrupt to PC through PCIE bus (for the edge interrupt, you need to memorize it to the interrupt activation status bit).
③ PC accesses to the interrupt service of CH367.
④ Interrupt service handles the necessary interrupts. This step can be re-executed before exiting the interrupt.
⑤ For the level interrupt, the interrupt service shall notify the external circuit to cancel the interrupt request.
⑥ For the edge interrupt, the interrupt service must clear the interrupt active status bit to 0.
⑦ CH367 cancels the interrupt request to the PC through PCIE bus.
⑧ After the interrupt processing is completed, the PC will exit the interrupt service of CH367.

6.6. Example Description

Designing a PCIE board card similar to the printer port based on CH367. The design stipulates that the I/O offset address 00H of the board is the data port, the offset address 01H is the status port, and the offset address 02H is the control port. When it is inserted into a PC, the board card may be assigned with an I/O base address 9500H, then the actual I/O address of the data port is 9500H, the I/O address of the status port is 9501H, and the I/O address of the control port is 9502H. Distinction of each port is achieved by address decoding of A7~A0 of CH367. If other ports are not required, only A1~A0 can be simplified decoding.

If two identical boards are inserted into the PC, the second board card will also be automatically assigned with an I/O base address by the system, but it will not be the same as the I/O base address of the first board card. If I/O base address of the second board card is C700H, actual I/O address of the control port of the second board card is C702H, so that two identical PCIE board cards have different I/O port addresses, avoiding I/O address conflicts.

The board card designer and related application know the offset address of each port in advance, but they

cannot know the I/O base address of the board card in advance, so the application needs to know the I/O base address of current board card through the I/O base address register of configuration space of the board card before the application performs I/O operation on the PCIE board card. Then, calculating the actual I/O address of each port is the I/O base address plus the offset address of each port. Finally, according to the actual I/O address, performing I/O operation on each port.

The following is an example of corresponding reading and writing process.

① Writing data 5AH to the control port, which is correspond to the C language program "outportb (IoBase+2,0x5A)", the variable IoBase is equal to the actual base address 0x9500 automatically assigned by the system. After execution, the address lines A7~A0 of CH367 output the offset address 02H of the control port (address 9502 is decomposed into base address 9500H and offset address 02H, and CH367 only outputs the offset address, not base address). CH367 data lines D7~D0 output 5AH, meanwhile, IOWR outputs a low-level pulse. The pulse width is pre-set by the read and write speed control register of CH367, and the default is 240nS.

② Reading data from the data port and status port, which is correspond to the C language program "inport (IoBase+0)". The low byte of the returned result which is the data read from the data port, and the high byte which is the data read from the status port. After execution, the address lines A7~A0 of CH367 firstly output the offset address 00H of the data port. Meanwhile, IORD outputs the first low-level pulse. The external device shall output data to the data buses D7~D0; then, the address lines A7~A0 of CH367 shall output the offset address 01H of status port. Meanwhile, IORD shall output the second low-level pulse. The external device shall output the data onto the date buses D7~D0.

6.7. Other Application Description

The RSTO pin of CH367 is reset output and is active at low level. During system reset, RSTO outputs low level; after the SPI interface FlashROM loads configuration information, RSTO outputs high level; then the IIC interface EEPROM loads configuration information; finally CH367 enters the normal working status, RSTO switches to general output pin.

The GPO pin of CH367 is the general output. During system reset, GPO outputs high level; meanwhile, checks the status of the general input pin GPI1. Before the reset is completed and SPI interface FlashROM configuration information is loaded, the GPO will be reconfigured according to the status of GPI1. If GPI1 is high during reset, GPO will remain to be at a high level; if GPI1 is low during reset, GPO will be switched to low level; finally, CH367 enters the normal operating status, GPO pin as the ordinary general output pin.

CH367 provides a hardware timing unit (SPICR[3:0]+CNTR) with a width of 12 bits. The timing is inputted based on the fractional frequency 204.8 of PCIE bus basic frequency. For the standard 100MHz basic frequency of PCIE bus, one count is increased for the hardware cycle count register every 2.048uS. The time from 000H to 0FFFH then from 0FFFH to 000H is totally 8388.608uS. By comparing the difference between two counts, the actual delay can be calculated to replace the computer software command cycle with large error.

Output pins of CH367 are all 3.3V LVCMOS levels, compatible with 5V TTL level. The input pins except for PCIE signal pin and WAKIN# pin can endure 5V withstand voltage and are compatible with 5V CMOS levels, 3.3 V LVCMOS and 5V TTL and LVTTL levels.

7. Parameters

7.1. Absolute Maximum Ratings

(Critical state or exceeding maximum can cause chip to not work or even be damaged)

Name	Parameter Description	Min.	Max.	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage ambient temperature	-55	125	℃
VCC33	I/O supply voltage (VCC33 connects to power, GND to ground)	-0.4	4.2	V
VCC18 VCC18A	Core supply voltage (VCC18 connects to power, GND to ground) Transmission supply voltage (VCC18A connects to power, GND to ground)	-0.4	2.3	V
VIO	Voltage of PCIE signal and WAKIN# input or output pins	-0.4	VCC33+0.4	V
VIO5	Voltage of other input or output pins	-0.4	5.4V	V

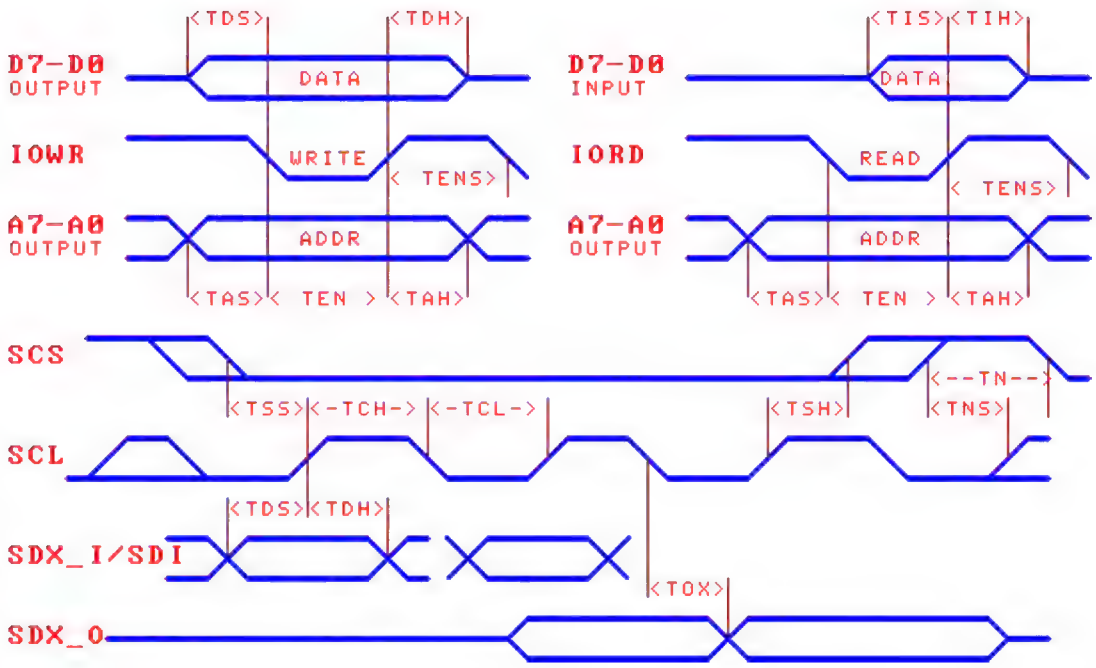
7.2. Electrical Parameters

(Test Conditions: TA=25℃, VCC33=3.3V, exclude pins connected to PCIE bus)

Name	Parameter Description	Min	Typ.	Max	Unit
VCC33	I/O supply voltage	3.0	3.3	3.6	V
VCC18 VCC18A	Core supply voltage Transmission supply voltage	1.65	1.8	1.95	V
ICC	Operating supply current (mainly in VCC18/A)		200	260	mA
VIL	Input low voltage	0		0.7	V
VIH	Input high voltage	2.0		VCC33	V
VOL4	Output low voltage of SDA pin (4mA draw current)			0.4	V
VOL	Output low voltage of other pin (6mA draw current)			0.4	V
VOH	Input high voltage (4mA output current)	VCC33-0.4			V
IIN	Input current of the input without pull-up			10	uA
IUP	Input current of the input with pull-up	20	40	100	uA

7.3. Timing Parameters

(Test Conditions: TA=25℃, VCC33=3.3V, refer to the figure)



Name	Parameter Description	Min	Typ.	Max	Unit
FCLK	CLK input frequency (basic frequency of PCIE bus)	0	100	105	MHz
FSCL2	SCL output frequency when the automatic loading of two-wire interface		244	260	KHz
FSCL3	SCL output frequency when the automatic loading of three-wire interface		31	35	MHz
TINTEG	Minimum pulse width of effective edge interrupt	5			nS
TEN	Low-level pulse width of IORD, IOWR read or write strobe	30	Optional 30~480	480	nS
TENS	High-level interval width of IORD, IOWR continuous strobes	90			nS
TAS	Address A7~A0 output building time	12	Optional 15 or 45		nS
TAH	Address A7~A0 output keeping time	12	Optional 15 or 45		nS
TDS	Data D7~D0 output building time	12	Optional 15 or 45		nS
TDH	Data D7~D0 output keeping time	12	Optional 15 or 45		nS
TIS	Data D7~D0 input building time	10			nS
TIH	Data D7~D0 input keeping time	0			nS
TSS	Effective building time of SCS before SCK rising edge	11	16 or 32		nS
TSH	Effective keeping time of SCS after SCK rising edge	11	16 or 32		nS

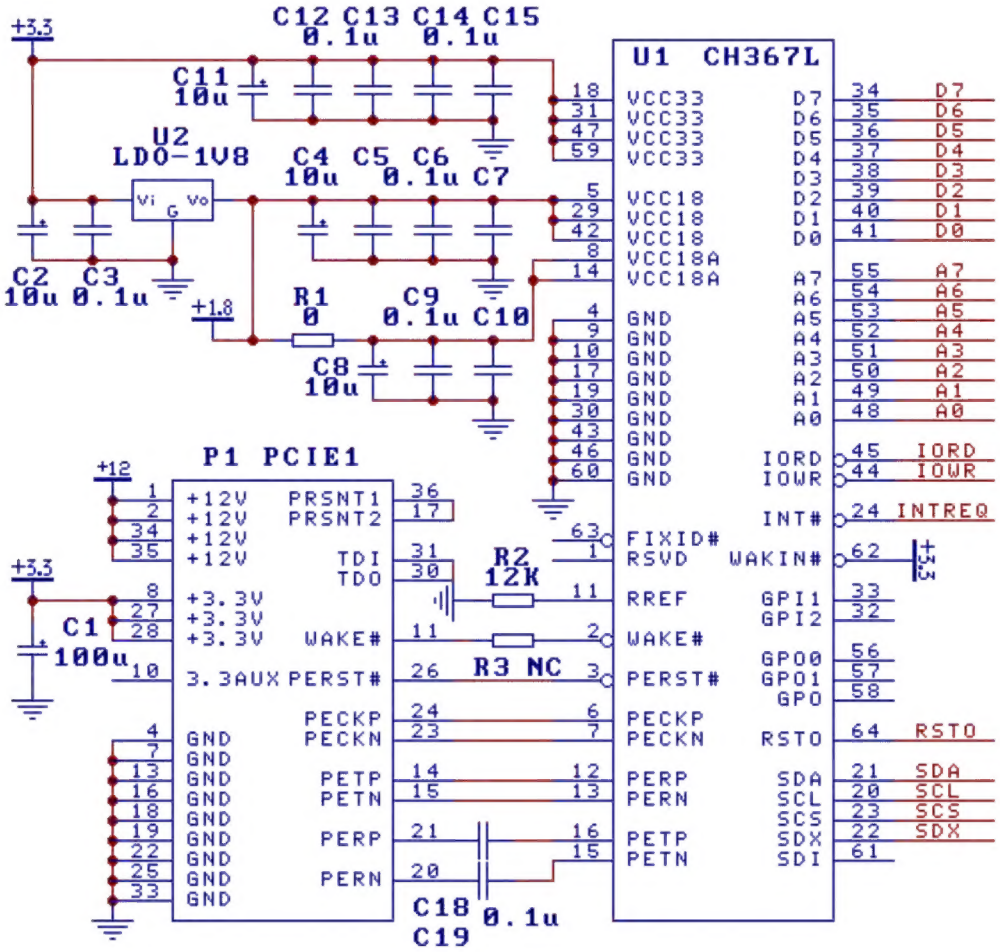
TNS	Ineffective building time of SCS before SCK rising edge	10			nS
TN	Ineffective time of SCS (SPI operation interval time)	110			nS
TCH	High-level time of SCK clock	13	16 or 32		nS
TCL	Low-level time of SCK clock	13	16 or 32		nS
TDS	SDX/SDI input building time before SCK rising edge	5			nS
TDH	SDX/SDI input keeping time after SCK rising edge	0			nS
TOX	SCK falling edge to Effective output or change of SDX	0	2	5	nS

8. Applications

8.1. Connect to PCIE Bus

This is the basic circuit that CH367 connects to PCIE bus.

The capacitor in the figure is used for power decoupling. The capacitor with a capacity of 10uF is a tantalum capacitor, and the capacitor with a capacity of 0.1uF is a monolithic or high-frequency ceramic capacitor, which are connected in parallel nearby to the power pins of CH367 respectively. LDO step- down device U2 must support 200mA current, and DC/DC can also be used instead.



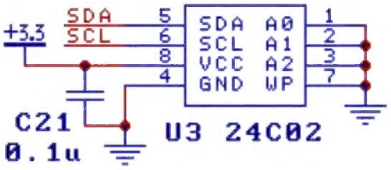
If the wake-up function is not used, it can remove R3 and make WAKE# pin suspended, but WAKIN# pin is

still connected with a high level.

CH367 is a high frequency circuit. Please refer to PCIE bus specification or PCIE_PCB.PDF document when designing the PCB board.

8.2. Connect to Configuration Chip

CH367 supports external EEPROM configuration chip 24CXX, which is used to provide identification information of PCIE board card such as VID/DID.



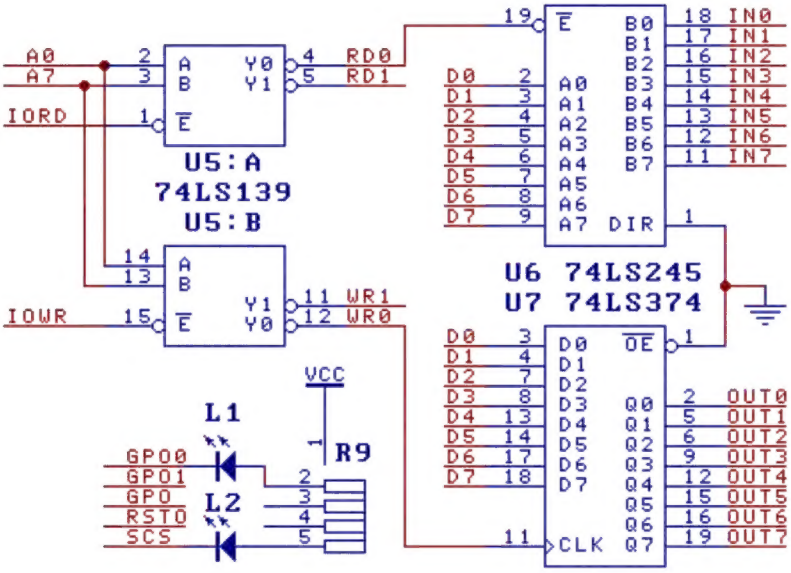
8.3. I/O Application

Read strobe/enable IORD and write strobe/enable IOWR control the decode enabling of 74LS139. 74LS139 makes that the address decoding outputs 2 paths of reading control and 2 paths of writing control. Through the 74LS245 inputs buffer and 74LS374 latch output to get 2 groups with 8-bit buffer input in each group and 2 groups with 8-bit latch output in each group. For example, if I/O base address of CH367 is set to 5A00H, then reading the 5A00H port means reading the first group of buffer input, and writing 5A01H port means writing the second group of latched output.

The above circuit can be replaced by a piece of CH351 to achieve 32 expanded bi-directional GPIO. Refer to CH351DS3 datasheet.

The general output pins GPO0, GPO1, GPO and RSTO and unused SCS can all be used as control outputs. GPO0 and GPO1 are at the low level by default after the system reset, and GPO is at the high level during reset, after reset, it is set by the input status of GPI1.

The drive current of CH367 output pin is greater than 5mA, and it can directly drive LED display after connecting with a current-limiting resistor in series. CH367 provides 8 address lines A7~A0 for I/O address decoding. The effective offset address range is 0EFH~00H, and the length is not greater than 232 bytes. Generally, external circuit does not require chip selection or directly forced.



The C-language WDM and DLL program based on CH367 for the above operations as follow:

```
UCHAR    mByte;
//Data unit, used to save data read from I/O port or to be written to I/O.
mPCH367_IO_REG     mIoBase;
// I/O port base address; the actual data unit address is equal to the base address plus the offset address.
CH367GetIoBaseAddr( &mIoBase );
// Gett the base address of I/O port, which is optional operation and not need to be executed.
// If not get I/O base address, only appointing the offset address in I/O operation, which means that I/O base address is 0.
// After calling the DLL of CH367, the DLL will automatically add the offset address to the base address and then perform I/O operation.
// The memory is similar to this. If only appointing the offset address in the memory operation, DLL will automatically add the memory base address
CH367ReadIoByte( & mIoBase -> mCH367_IOXR[0x00], &mByte );
// read one-byte data from 00H offset address of I/O port, namely, read the buffer input of first group.
CH367WriteIoByte( & mIoBase -> mCH367_IOXR[0x01], 0x47 );
// In the above operation, write the data 47H into the 01H offset address of the I/O port, namely, as the latch output of second group.
CH367WriteIoByte( & mIoBase -> mCH367_GPOR2, 0x02 );
// Set GPO0 at low level, GPO1 at high level, and GPO at low level
```

In DOS or PC without OS, the assembly program for the above operation is:

```
MOV   AX, 0B109H                  ; read PCIE configuration space in the unit of character
MOV   BX, CH367_PCIE_BUS_DEV_ADDR ;PCIE address of CH367 board card, namely, bus/device/function number
MOV   DI, 0010H                   ;offset address PC_BASE_ADDR0 of I/O port base address register
INT   1AH                         ; read the base address of I/O port, automatically set when the PC is initialized
AND   CX, 0FFFEH                  ; get the base address of I/O port; the lowest bit is indication bit, shielded
MOV   BX, CX                      ; this value is the base address of I/O port
LEA   DX, [BX].CH367_IOXR[0]      ; I/O port address of the buffer inputs of first group, I/O base address plus 0
IN    AL, DX                      ; read the buffer input data of 74LS245
LEA   DX, [BX].CH367_IOXR[1]      ; I/O port address of latch output of the second group, I/O base address plus 1
MOV   AL, 47H
OUT   DX, AL                      ; write the data 47H into 74LS374 latch output register
LEA   DX, [BX].CH367_GPOR2        ; I/O port address of general output register 2, inside CH367
IN    AL, DX                      ; for maintaining the status of the other pins, firstly read the original GPO pin status
OR    AL, 02H                     ; only set GPO1 at high level, the other pins keep unchanged
AND   AL, 0FEH                    ; only set GPO0 at low level, the other pins keep unchanged
OUT   DX, AL                      ; write new GPO into general output register 2
```

8.4. Connect to MCU, etc.

PC makes bi-directional data transmission through CH367 and MCU or DSP. There are three methods: Firstly, using the dual-port SRAM to enable CH367 and MCU to write and read the same memory, and the bi-directional data exchange is made in the unit of big data block; secondly, using the bi-directional buffer interface chip CH421 to provide a 64-byte buffer for CH367 and MCU to write to each other respectively,

and the bi-directional data exchange is made in the unit of 64-byte data blocks; thirdly, using SPI host interface of CH367 or UART of CH382 to exchange data in the unit of byte without additional hardware costs.